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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,941	10/31/2003	Toru Takayama	0756-7215	8929

31780 7590 05/09/2006

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EXAMINER

NGUYEN, JOSEPH H

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 05/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/697,941

Applicant(s)

TAKAYAMA ET AL.

Examiner

Joseph Nguyen

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 31 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 4,5,20 and 28-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 4,5,20 and 28-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui (US 6,900,861) in view of Choi et al. (US 2002/0084459)

Regarding claim 4, Yasui discloses in figure 3 a semiconductor device comprising a substrate 10A (col. 8, lines 38-39); an adhesive material 10B (col. 9, lines 29-30) over the substrate; a protective film 12 (col. 9, lines 30-32) over the adhesive material; an insulating film 206b (col. 10, line 20) over the protective film; and a thin film transistor 30 (col. 9, line 65) over the insulating film. Yasui further discloses the protective film 12 is formed of silicon oxide (col. 13, lines 46-48), but not of Teflon as claimed. However, Choi et al. discloses in para [0062] the protective film 48 can be formed of silicon oxide or Teflon. In view of such teaching, it would have been obvious at the time of the present invention to modify Yasui by substituting Teflon for silicon oxide to form a protective film because Teflon and silicon oxide were art equivalents recognized.

Regarding claim 5, Yasui discloses the semiconductor device is a personal computer as shown in figure 19.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui in view of Shimoda et al. (US 2006/0030122) and further in view of Arao et al. (US 2002/0016028).

Regarding claim 20, similar to claim 4 above, Yasui discloses in figure 3 substantially all the structure set forth in claim 20 except a battery over the substrate. However, Shimoda et al. discloses in para [0359] and figure 35(a) a battery 340 over the substrate 182. In view of such teaching, it would have been obvious at the time of the present invention to modify Yasui by having a battery over the substrate along with other semiconductor elements such that the simplification and miniaturization of a semiconductor device can be obtained.

Further, Yasui and Shimoda et al. do not disclose the central processing unit including a thin film transistor of n channel type and a thin film transistor of p channel type. It is noted that Yasui discloses in figures 1 and 3 a central processing unit comprising a control section 30, an operation section 9a, 16 and a memory unit 70, 3b, 6a over the insulating film 206b (See col. 7). However, Arao et al. discloses in figure 19B the central processing unit including a thin film transistor of n channel type 601 and a thin film transistor of p channel type 602. In view of such teaching, it would have been obvious at the time of the present invention to modify Yasui and Shimoda et al. by having the central processing unit including a thin film transistor of n channel type and a thin film transistor of p channel type (CMOS) to improve the driver circuit since the CMOS driver circuit is more efficient to drive the liquid crystal device.

Claims 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui in view of Shimoda et al. and in view of Choi et al. and further in view of Arao et al.

Regarding claims 28-29, similar to claim 20 above, Yasui discloses in figure 3 substantially all the structure set forth in claims 28-29 except the substrate being plastic and a battery over the substrate. However, Shimoda et al. discloses in para [0359] and figure 35(a) the substrate 182 being plastic and a battery 340 over the substrate 182. In view of such teaching, it would have been obvious at the time of the present invention to modify Yasui by having the substrate being plastic and a battery over the substrate along with other semiconductor elements such that the simplification and miniaturization of a semiconductor device can be obtained.

Further, Yasui further discloses the protective film 12 is formed of silicon oxide (col. 13, lines 46-48), but not of Teflon as claimed. However, Choi et al. discloses in para [0062] the protective film 48 can be formed of silicon oxide or Teflon. In view of such teaching, it would have been obvious at the time of the present invention to modify Yasui and Shimoda et al. by substituting Teflon for silicon oxide to form a protective film because Teflon and silicon oxide were art equivalents recognized.

Lastly, Yasui and Shimoda et al. and Choi et al. do not disclose the central processing unit including a thin film transistor of n channel type and a thin film transistor of p channel type. However, Arao et al. discloses in figure 19B the central processing unit including a thin film transistor of n channel type 601 and a thin film transistor of p

channel type 602. In view of such teaching, it would have been obvious at the time of the present invention to modify Yasui and Shimoda et al. and Choi et al. by having the central processing unit including a thin film transistor of n channel type and a thin film transistor of p channel type (CMOS) to improve the driver circuit since the CMOS driver circuit is more efficient to drive the liquid crystal device.

Regarding claims 30-31, Yasui discloses the semiconductor device is a personal computer as shown in figure 19.

### ***Response to Arguments***

Applicant's arguments filed on 03/31/2006 have been fully considered but they are not persuasive.

With respect to claims 28-29, Applicant argues the protective layer 48 of Choi et al. is not formed between a thin film transistor and the substrate recited in claims 28-29. However, Yasui discloses in figure 3 the protective film 12 is formed between a thin film transistor 30 and the substrate 10A. Also, Yasui's protective film is formed of silicon oxide, not Teflon as claimed, and Choi et al. teaches the protective film can be formed of silicon oxide or Teflon. In other words, Teflon and silicon oxide were art equivalents recognized to form a protective film. As such, the combination of Yasui and Choi et al. would teach or suggest all the claim limitations recited in claims 28-29 herein.

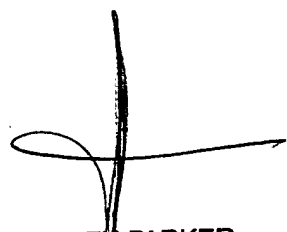
Applicant's arguments with respect to claims 4-5, 20, 28-31 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN  
May 4, 2006.



KENNETH PARKER  
SUPERVISORY PATENT EXAMINER